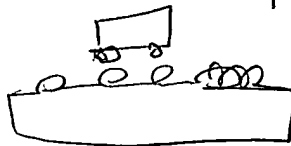


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For the S P R / primary  
reference 16.5.01  
16.4.02

Serial No. 09/944,487

IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A method for interconnecting at least two semiconductor dice, comprising:  
providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;  
providing at least one second semiconductor die including a plurality of bond pads on an active surface thereof;  
orienting the first semiconductor die and the at least one second semiconductor die with the active surfaces thereof facing each other by aligning a peripheral edge of the at least one second semiconductor die with an alignment structure disposed on the active surface of the first semiconductor die and interacting with the peripheral edge of the at least one second semiconductor die, the at least one second semiconductor die covering some bond pads of the plurality of bond pads, other bond pads of the plurality of bond pads remaining exposed beyond an outer periphery of the at least one second semiconductor die;  
electrically connecting the some bond pads with corresponding bond pads of the plurality of bond pads of the first semiconductor die.

2. (Previously presented) The method of claim 1, wherein providing the first semiconductor die comprises providing a logic device.

3. (Previously presented) The method of claim 2, wherein providing the at least one second semiconductor die comprises providing at least one memory device.

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4. (Previously presented) The method of claim 1, wherein electrically connecting comprises providing conductive structures directly between each of the plurality of bond pads of the at least one second semiconductor die and the corresponding bond pads of the first semiconductor die.

5. (Previously presented) The method of claim 4, wherein providing conductive structures comprises providing balls, bumps, columns, or pillars comprising conductive material.

6. (Previously presented) The method of claim 4, wherein providing conductive structures comprises providing structures formed from a material comprising at least one of a metal, an alloy, a conductive epoxy, and a conductor-filled epoxy.

7. (Previously presented) The method of claim 1, further comprising aligning the at least some bond pads of the at least one second semiconductor die with the corresponding bond pads of the first semiconductor die.

8. (canceled)

9. (Previously presented) The method of claim 1, further comprising:  
providing a carrier including a plurality of contacts;  
orienting the first semiconductor die with the active surface thereof facing the carrier; and  
electrically connecting the other bond pads of the first semiconductor die to corresponding contacts of the carrier.

10. (Previously presented) The method of claim 9, wherein providing the carrier comprises providing a carrier substrate with the plurality of contacts comprising contact pads located on a surface thereof.

11. (Previously presented) The method of claim 10, wherein providing the carrier substrate comprises providing the carrier substrate with at least one recess formed in the surface.

12. (Previously presented) The method of claim 11, wherein orienting includes at least partially disposing at least the at least one second semiconductor die in the at least one recess.

13. (Previously presented) The method of claim 9, wherein providing the carrier comprises providing leads corresponding to each of the other bond pads.

14. (Previously presented) The method of claim 9, wherein electrically connecting the other bond pads of the first semiconductor die to the corresponding contacts of the carrier comprises disposing conductive elements between the other bond pads and the corresponding contacts.

15. (Previously presented) The method of claim 14, wherein disposing conductive elements comprises providing at least one of balls, bumps, columns, and pillars comprising conductive material between each of the other bond pads and the corresponding contacts.

16. (Previously presented) The method of claim 14, wherein disposing the conductive elements between the other bond pads of the first semiconductor die and the corresponding contacts of the carrier comprises providing a quantity of a material comprising at least one of a metal, an alloy, a conductive epoxy, and a conductor-filled epoxy.

17. (Previously presented) The method of claim 10, wherein providing the first semiconductor die comprises providing the first semiconductor die with a first member of a conductive element secured to each other bond pad thereof and wherein providing the carrier substrate comprises providing the carrier substrate with a second member of the conductive element secured to each corresponding contact pad thereof.

18. (Previously presented) The method of claim 17, further comprising aligning at least the first and second members of the conductive element.

19. (Previously presented) The method of claim 18, further comprising securing at least the first and second members of the conductive element directly to each other.

20. (Previously presented) The method of claim 17, further comprising providing a conductive mating structure bearing a third member of the conductive element between the first semiconductor die and the carrier substrate.

21. (Previously presented) The method of claim 20, further comprising aligning the first, second, and third members of the conductive element.

22. (Previously presented) The method of claim 21, further comprising securing the first, second, and third members of the conductive element to one another.

23. (Currently amended) A method for packaging a semiconductor device assembly, comprising:  
providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;  
providing at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof;  
orienting the at least one second semiconductor die over the first semiconductor die with the active surface facing the active surface of the first semiconductor die by aligning a peripheral edge of the at least one second semiconductor die with an alignment structure disposed on the active surface of the first semiconductor die and interacting with the peripheral edge of the at least one second semiconductor die, the corresponding bond

pads of the first and the at least one second semiconductor dice in alignment with one another;  
electrically connecting at least some bond pads of the corresponding bond pads via laterally discrete, physically unconnected conductive structures;  
electrically connecting bond pads of the first semiconductor die exposed beyond the outer periphery of the at least one second semiconductor die to the corresponding contacts of the carrier;  
providing a carrier with a plurality of contacts; and  
orienting the first semiconductor die over the carrier with the active surface facing the carrier, bond pads of the first semiconductor die exposed beyond an outer periphery of the at least one second semiconductor die in alignment with corresponding contacts of the carrier.

24. (Previously presented) The method of claim 23, further comprising electrically connecting the plurality of bond pads of the at least one second semiconductor die to the corresponding plurality of bond pads of the first semiconductor die.

25. (canceled)

26. (Previously presented) The method of claim 23, further comprising disposing a quantity of encapsulant material over at least the active surface of the first semiconductor die.

27. (Previously presented) The method of claim 26, wherein disposing the quantity of encapsulant material comprises disposing underfill material between the first semiconductor die and the carrier.

28. (Previously presented) The method of claim 26, wherein disposing the quantity of encapsulant material comprises substantially covering at least the first semiconductor die.

29. (Previously presented) The method of claim 23, wherein providing the carrier comprises providing a carrier substrate with the plurality of contacts comprising contact pads located on a surface thereof.

30. (Previously presented) The method of claim 29, wherein providing the carrier substrate comprises providing a carrier substrate with at least one recess formed in the surface.

31. (Previously presented) The method of claim 30, wherein orienting the first semiconductor die comprises at least partially disposing the at least one second semiconductor die within the at least one recess.

32. (Previously presented) The method of claim 23, wherein providing the carrier comprises providing a plurality of leads, each of the plurality of leads corresponding to the bond pads of the first semiconductor die exposed beyond the outer periphery of the at least one second semiconductor die.

33. (Previously presented) The method of claim 29, wherein:  
the providing the first semiconductor die comprises providing the first semiconductor die with a first member of a conductive element secured to each bond pad thereof that is located beyond the outer periphery of the at least one second semiconductor die; and  
the providing the carrier substrate comprises providing the carrier substrate with a second member of the conductive element secured to each corresponding contact pad thereof.

34. (Previously presented) The method of claim 33, further comprising aligning at least the first and second members of the conductive element.

35. (Previously presented) The method of claim 34, further comprising securing at least the first and second members of the conductive element directly to each other.

36. (Previously presented) The method of claim 33, further comprising providing a conductive mating structure bearing a third member of the conductive element between the first semiconductor die and the carrier substrate.

37. (Previously presented) The method of claim 36, further comprising aligning the first, second, and third members of the conductive element.

38. (Previously presented) The method of claim 37, further comprising securing the first, second, and third members of the conductive element to one another.

39. (Currently amended) A method for packaging a semiconductor device assembly, comprising:

providing at least a first multi-chip module including:

a first semiconductor die with a plurality of bond pads arranged in an array over an active surface thereof; and

at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof, at least one peripheral edge of the at least one second semiconductor die aligned with an alignment structure disposed on the active surface of the first semiconductor die and interacting with the at least one peripheral edge of the at least one second semiconductor die, each of the plurality of bond pads of the at least one second semiconductor die in alignment with corresponding bond pads of the first semiconductor die, other bond pads of the first semiconductor die being exposed beyond an outer periphery of the at least one second semiconductor die, the active surfaces of the first semiconductor die and the at least one second semiconductor die facing one another, and the bond pads of the at least one second semiconductor die electrically connected to the corresponding bond pads of the first semiconductor die, other bond pads of the

first semiconductor die exposed laterally beyond an outer periphery of the at least one second semiconductor die;  
providing a carrier including contacts; and  
orienting the at least the first multi-chip module with the active surface of the first semiconductor die facing the carrier and the other bond pads in alignment with corresponding contacts of the carrier.

40. (Previously presented) The method of claim 39, further comprising:  
providing at least a second multi-chip module including:  
another first semiconductor die with a plurality of bond pads arranged in an array over an active surface thereof; and  
an another at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof, each of the plurality of bond pads of the another at least one second semiconductor die in alignment with corresponding bond pads of the another first semiconductor die, the active surfaces of the another first semiconductor die and the another at least one second semiconductor die facing one another, and the bond pads of the another at least one second semiconductor die electrically connected to the corresponding bond pads of the another first semiconductor die, other bond pads of the another first semiconductor die exposed laterally beyond an outer periphery of the another at least one second semiconductor die; and  
orienting the another at least the second multi-chip module over the carrier with the active surface of the another first semiconductor die facing the carrier and the other bond pads in alignment with corresponding contacts of the carrier.



41. (Previously presented) The method of claim 12, further comprising:  
positioning a cover over the first semiconductor device and the at least one second  
semiconductor device.

42. (Previously presented) The method of claim 1, wherein at least one of providing the  
first semiconductor die and providing the at least one second semiconductor die comprises  
providing at least one semiconductor die with at least some of the bond pads thereof being  
exposed through alignment recesses in an active surface thereof.

43. (Previously presented) The method of claim 39, wherein:  
providing the carrier comprises providing a carrier including a recess with a ledge therein and  
contacts exposed at the ledge; and  
orienting comprises orienting the at least the first multi-chip module within the recess with the  
active surface of the first semiconductor die facing the carrier and the ledge.

44. (Previously presented) The method of claim 43, further comprising:  
positioning a cover over the recess and the first and at least one second semiconductor dice  
therein.